

Docket No.: 4363P004

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IDS
Y. K. Lim
7/25/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

ARASHI HASSIBI, ET AL.

Application No.: 09/843,486

Filed: April 25, 2001

For: **Optimal Simultaneous Design and
Floorplanning of Integrated Circuit**

Art Group: 2811

Examiner: Quang D. Vu

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted before the mailing of a final Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Copies of the references cited on PTO/SB/08 are enclosed herewith.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

The fee set in the amount of \$180.00 for submission of the Information Disclosure Statement is enclosed herewith. Please charge any additional fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SKOLOFF, TAYLOR & ZAFMAN LLP

Date: _____

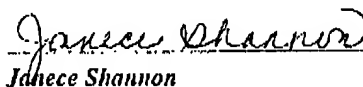
7/11/03



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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Janece Shannon

7-11-2003

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Date